-- LAB8\_PRELAB.asm

-- This assembly code produces D = (A AND B) XOR C

-- Leo Weng

-- ECE 2031 L01

-- 10/31/2016

ORG 0

Start: CALL CALC

JUMP Start

ORG &H010

CALC: LOAD A

AND B

XOR C

STORE D

RETURN

ORG &H030

A: DW &H00FF ;A

B: DW &HA5A5 ;B

C: DW &H3300 ;C

D: DW &H0005 ;D

**Figure 1.** The assembly code creates a subroutine CALC that performs .

-- LAB8\_PRELAB.mif

-- This mif file produces D = (A AND B) XOR C

-- Leo Weng

-- ECE 2031 L01

-- 10/31/2016

DEPTH = 1024;

WIDTH = 16;

ADDRESS\_RADIX = HEX;

DATA\_RADIX = HEX;

CONTENT

BEGIN

[000..3FF] : 0000; -- Default to NOP

000 : 4010; -- Start: CALL CALC

001 : 1400; -- JUMP Start

010 : 0430; -- CALC: LOAD A

011 : 2431; -- AND B

012 : 2C32; -- XOR C

013 : 0833; -- STORE D

014 : 4400; -- RETURN

030 : 00FF; -- A: DW &H00FF ;A

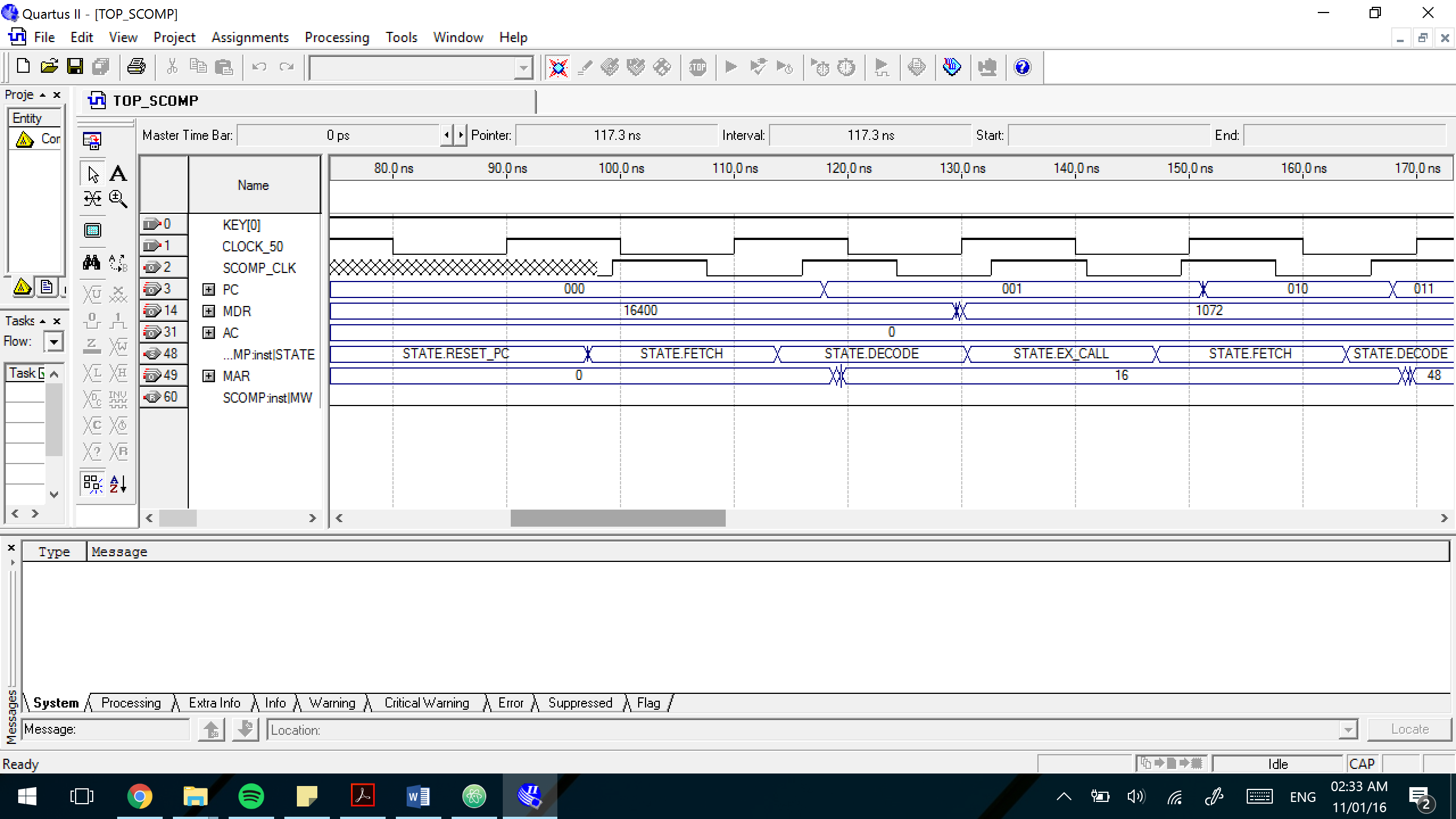
031 : A5A5; -- B: DW &HA5A5 ;B

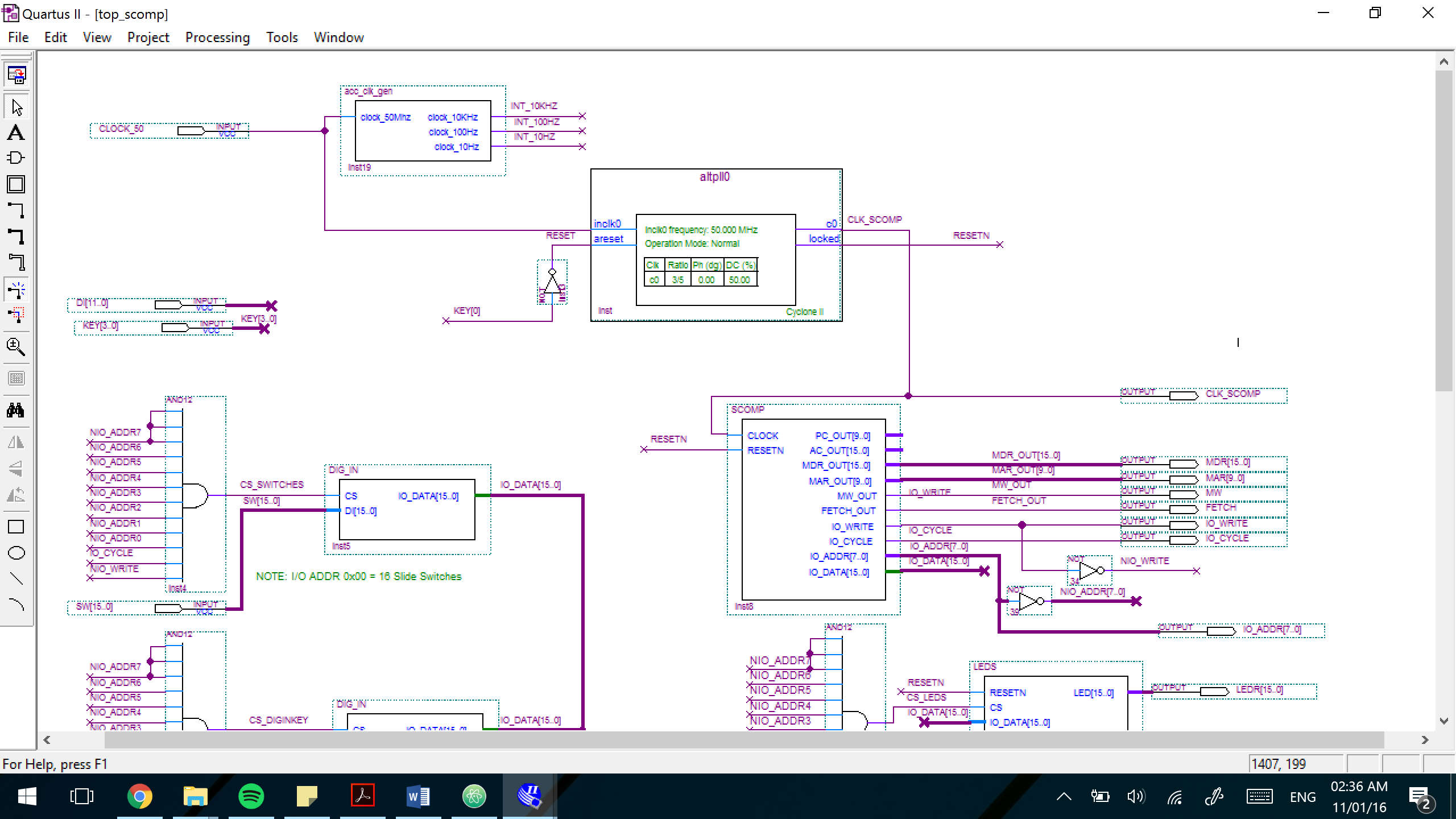
032 : 3300; -- C: DW &H3300 ;C

033 : 0005; -- D: DW &H0005 ;D

END;

**Figure 2.** The .mif file is generated from the .asm code from Figure 1 and performs .



**Figure 3.** The timing simulation waveform for the Simple Computer computing and implementing LAB8\_PRELAB.MIF. The partial simulation results show the signals needed to verify proper operation of the instructions.

**Figure 4.** Part of the schematic diagram TOP\_SCOMP.BDF, showing the connected clock signal from PLL to SCOMP.

-- LAB8.asm

-- This assembly code displays the value of the slide switches for two seconds then shifts left

-- Leo Weng

-- ECE 2031 L01

-- 10/31/2016

ORG 0

IN SWITCHES

STORE INDATA

Halp: OUT LEDS

OUT SEVENSEG

SHIFT 1

STORE INDATA

OUT TIMER

Wait: IN TIMER

ADDI -20

JNEG Wait

LOAD INDATA

JUMP Halp

SWITCHES: EQU &H00

LEDS: EQU &H01

TIMER: EQU &H02

SEVENSEG: EQU &H04

INDATA: DW &H0000

**Figure 5.** The assembly code implements IN, OUT, and SHIFT to display the value of the slide switches for two seconds then shifts left one bit.

-- LAB8.mif

-- This mif file displays the value of the slide switches for two seconds then shifts left

-- Leo Weng

-- ECE 2031 L01

-- 10/31/2016

DEPTH = 1024;

WIDTH = 16;

ADDRESS\_RADIX = HEX;

DATA\_RADIX = HEX;

CONTENT

BEGIN

[000..3FF] : 0000; -- Default to NOP

000 : 4800; -- IN SWITCHES

001 : 080C; -- STORE INDATA

002 : 4C01; -- Halp: OUT LEDS

003 : 4C04; -- OUT SEVENSEG

004 : 3001; -- SHIFT 1

005 : 080C; -- STORE INDATA

006 : 4C02; -- OUT TIMER

007 : 4802; -- Wait: IN TIMER

008 : 37EC; -- ADDI -20

009 : 1807; -- JNEG Wait

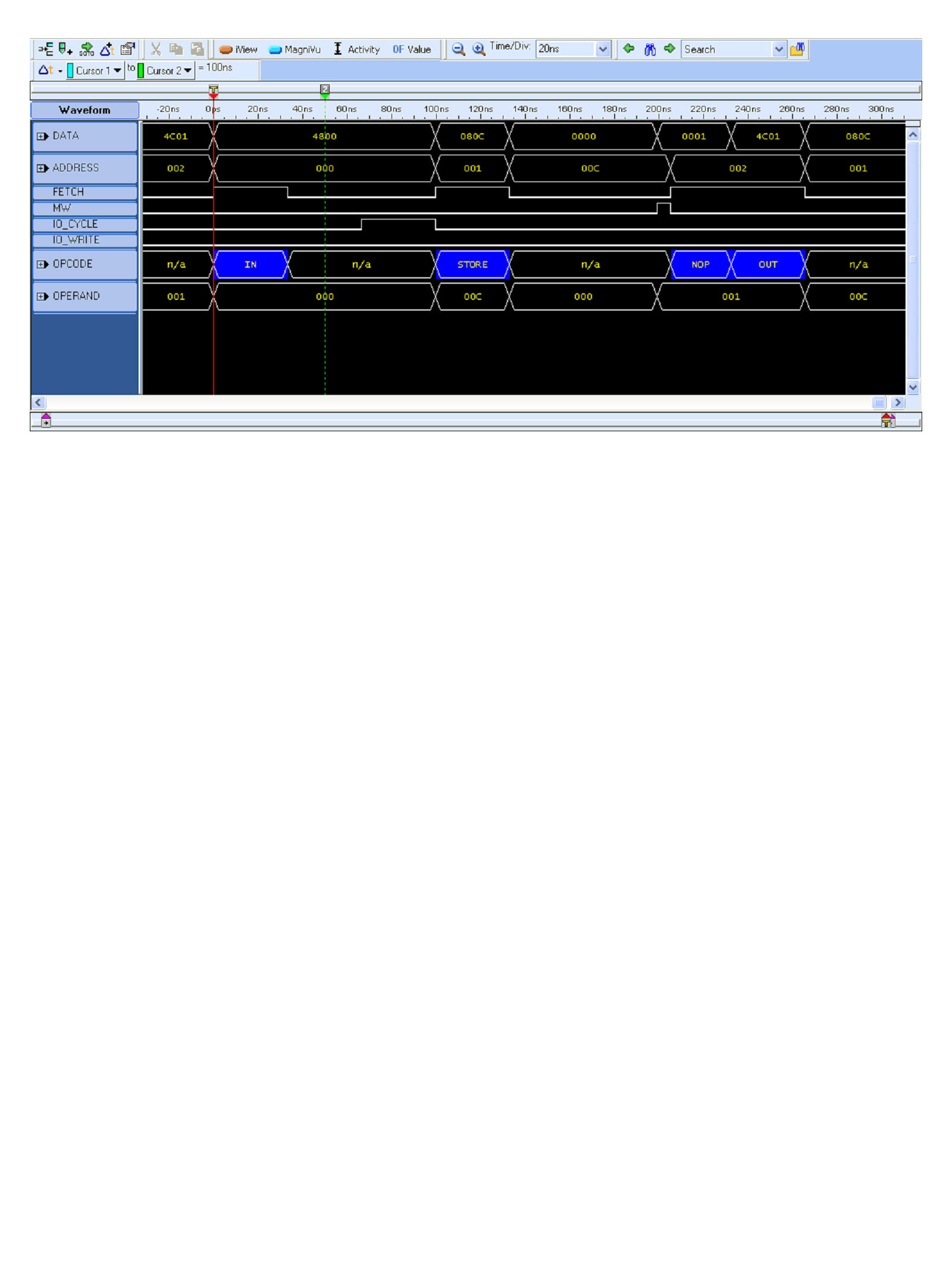
00A : 040C; -- LOAD INDATA

00B : 1402; -- JUMP Halp

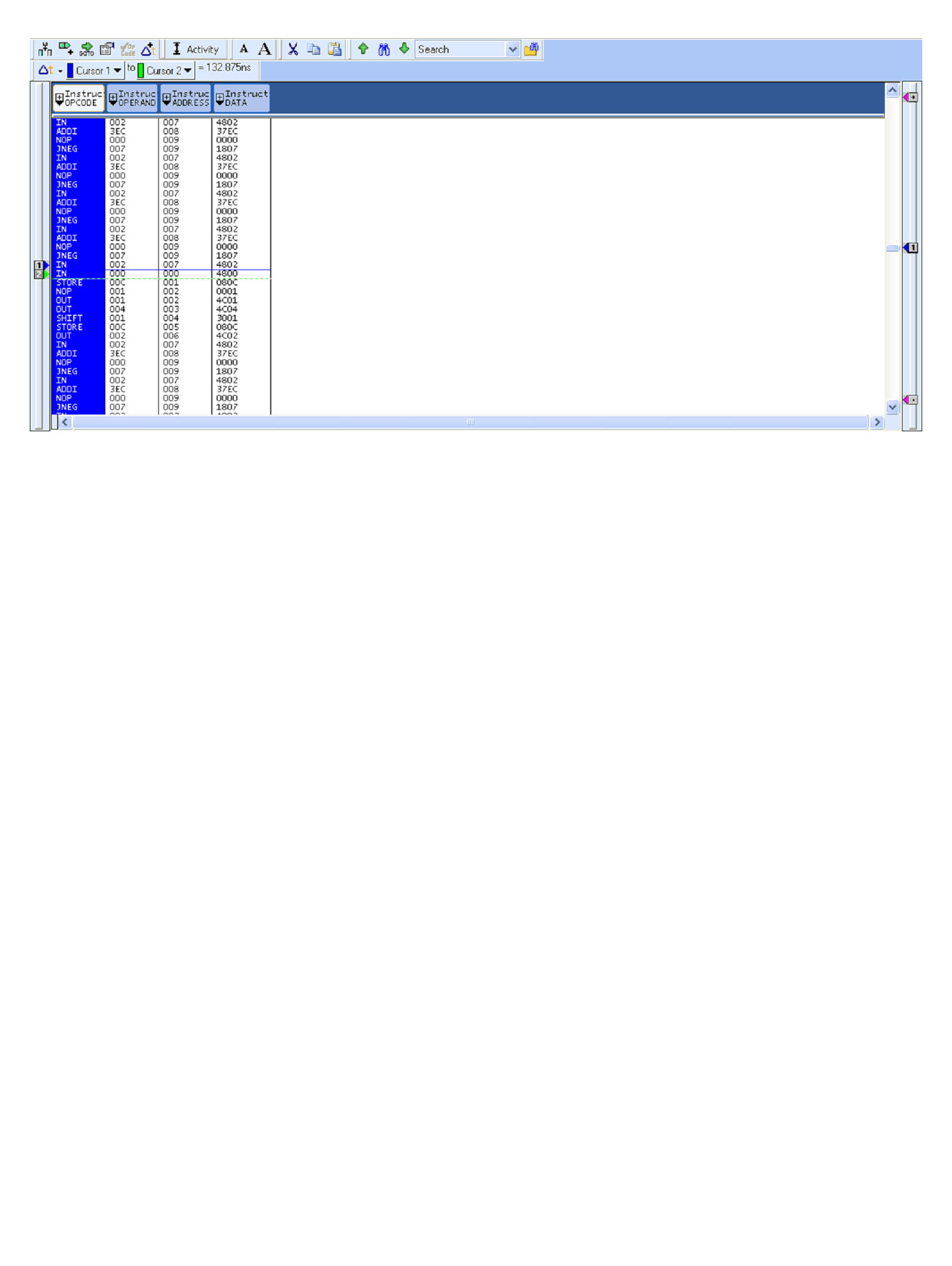
00C : 0000; -- INDATA: DW &H0000

END;

**Figure 6.** The mif file is generated from the assembly code in Figure 5. The program displays the value of the slide switches for two seconds then shifts left one bit.



**Figure 7.** Screen capture from logic analyzer showing a disassembled waveform. The trigger (T) indicates the beginning of the program: the instruction (OPCODE) IN corresponds with DATA address 4800, which can be verified with Figure 6 as well.



**Figure 8.** Screen capture from logic analyzer showing a disassembled listing. The trigger (1) indicates the beginning of the program: the instruction (OPCODE) IN corresponds with DATA address 4800, which can be verified with both Figure 6 and Figure 7.